AMENDMENTS TO THE CLAIMS

1. (Original) A method for time multiplexing signals comprising:

merging a set of nets carrying the signals into a shared interconnect portion;

altering a netlist based on the merging; and

placing a design represented by the altered netlist.

2. (Original) A method of time multiplexing signals on interconnect in a programmable logic device, the method comprising:

merging the nets into a shared interconnect portion;

altering the design based on the merging;

placing the altered design; and

routing the altered design.

3. (Currently Amended) An integrated circuit comprising:

a set of configurable logic blocks comprising multiple signal sources and at least one destination; [[and]]

a time multiplexing signal generator controlling which of the multiple signal sources provides its signal to a corresponding signal destination; and

a programmable interconnect coupled between the output of the time multiplexing signal generator and the destination configurable logic block.

4. (Original) The integrated circuit of Claim 1, wherein the multiple signal sources are located in one configurable logic block.

5. (Original) The integrated circuit of Claim 1, wherein the multiple signal sources generate critical signals.

6. (Original) The integrated circuit of Claim 1, wherein the time multiplexing signal generator includes a counter.

7. (New) The method of Claim 1, further comprising a step of analyzing nets for high latency signals.

8. (New) The method of Claim 7, further comprising a step of collecting the nets having high latency signals into shared interconnect groups.

9. (New) The method of Claim 1, wherein the altered netlist comprises a plurality of signal sources in the same configurable logic block.

10. (New) The method of Claim 1, further comprising a step of performing an initial routing of the set of nets.

11. (New) The method of Claim 10, further comprising a step of identifying nets comprising signal sources having associated programmable interconnects in substantially the same area.

12. (New) The method of Claim 2, wherein the altered design comprises a plurality of source configurable logic blocks and a plurality of destination configurable logic blocks.

13. (New) The method of Claim 12, further comprising a step of selecting a source configurable logic block by way of a multi-bit phase bus.

14. (New) The method of Claim 13, further comprising a step of allowing a destination configurable logic block to receive signals of any phase of said multi-phase bus.

15. (New) The method of Claim 12, further comprising a step of generating a clock signal comprising a global reset signal indicating a first phase to synchronize the plurality of source configurable logic blocks.

16. (New) The method of Claim 15, further comprising a step of separately detecting the current time multiplexed phase at each of the source configurable logic blocks and destination configurable logic blocks.

17. (New) The integrated circuit of Claim 3, further comprising a plurality of destinations within the destination configurable logic block, wherein the signal source of the multiple signal sources selected by the time multiplexing signal generator is coupled to one of the destinations within the destination configurable logic block.

18. (New) The integrated circuit of Claim 3, further comprising a plurality of destination configurable logic blocks.

19. (New) The integrated circuit of Claim 18, wherein the time multiplexing signal generator comprises a multiplexer coupled to the multiple signal sources and controlled by a time multiplexing signal.

20. (New) The integrated circuit of Claim 19, wherein each destination configurable logic block comprises a capture device coupled to receive the time multiplexing signal, wherein at least one configurable logic clock is coupled to receive a signal from the selected signal source based upon the time multiplexing signal.